

Allan J. Romeo

Medford, MA

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EDUCATION

Tufts University, Medford, MA

Expected May 2028

Bachelor of Science, Computer Engineering GPA: 3.6

Relevant Coursework: Computer Architecture, Embedded Systems, Machine Structure and Assembly Language Programming, Data Structures, Introduction to Machine Learning, Probabilistic Systems Analysis

TECHNICAL SKILLS

- **Languages:** Rust, C, C++, Python, x86 Assembly, Bash
- **Systems & Tools:** Git, GNU Make, GDB, Linux (Arch), tmux, L^AT_EX
- **Hardware / Embedded:** STM32 microcontrollers (Nucleo-32), SPI / I²C / UART protocols, GPIO, ADC, interrupt-driven firmware, OV2640 camera sensor, ST7789 display driver, SD card interface, PlatformIO
- **Architecture & Simulation:** ChampSim, LLC replacement policy design and analysis, performance counter analysis, trace-driven cache hierarchy modeling

RESEARCH PROJECT

LLC Replacement Policy Evaluation, Tufts University — EE156

2026

Collaborator: Luciano Galvani

- Compared six LLC replacement policies (LRU, SRRIP, DRRIP, SHiP, Hawkeye, Mockingjay) across 60+ benchmarks spanning SPEC CPU2006/2017, Google Workload Traces, and Ligra graph suites using the ChampSim simulation framework
- Identified systematic performance inversions in OPTgen-based policies (Hawkeye, Mockingjay) on branch-bound workloads, forming the central finding of a co-authored research paper
- Delivered findings as an IEEE-format two-column paper and a 15-slide technical presentation

PROJECTS

Aster — Cache Hierarchy Simulator, Rust

2026–present

- Built a trace-driven cache hierarchy simulator reading ChampSim-format memory traces, with a trait-based replacement policy system (LRU, SRRIP) validated for hit/miss-rate parity against ChampSim reference output
- Extended the hierarchy with a split L1 instruction cache alongside a shared L2/LLC, dirty-bit tracking with writeback propagation between cache levels, and a PC-keyed stream buffer prefetcher
- Designed the simulator around TOML-based configuration

Embedded Digital Camera, STM32L432 Nucleo-32 (PlatformIO / C)

2025

- Implemented bare-metal firmware integrating an OV2640 image sensor (SCCB/I²C), ST7789 SPI display, and SD card peripheral on a resource-constrained microcontroller
- Wrote register-level initialization sequences from datasheets, handled DMA-backed pixel transfer, and debugged signal integrity issues on a breadboarded prototype
- Managed competing peripheral timing constraints across SPI, I²C, and GPIO simultaneously

Universal Machine Emulator, C

2025

- Implemented a 14-instruction virtual machine in C, including memory segmentation, bitfield-encoded instruction decoding, and dynamic segment allocation
- Gained hands-on experience with low-level memory management and instruction set design

EXPERIENCE

Customer Service, Fruit and Salad Co.

March 2024–August 2025

- Managed customer orders and front-of-house operations under high-volume service conditions

Volunteer Assistant Rowing Coach

Summers 2021–2023

- Coached middle and early high school students across three summer seasons, delivering structured technical instruction to groups of varying skill levels
- Supported session planning, safety monitoring, and on-water logistics alongside lead coaches